PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

TAKAYAMA, SHUICHI, et al. : Confirmation Number: 9991

Application No.: 10/051,335 : Group Art Unit: 2191

Filed: October 19, 2001 : Examiner: Satish Rampuria

For: PROCESSOR FOR EXECUTING INSTRUCTIONS IN UNITS THAT ARE UNRELATED TO THE UNITS IN WHICH INSTRUCTIONS ARE READ, AND A COMPILIER, AN OPTIMIZATION APPARATUS, AN ASSEMBLER, A LINKER, A DEBUGGER AND A DISASSEMBLIER FOR SUCH PROCESSOR

INFORMATION DISCLOSURE STATEMENT

Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

10/051,335

Each non-English language reference (translations attached) was first cited in a corresponding foreign application office action and its relevance discussed therein. A copy of the foreign office action, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Please recognize our Customer No. 20277

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WDC99 1124987-1.067471.0017

SHEET 1 OF 1 INFORMATION DISCLOSURE SERIAL NO. ATTY. DOCKET NO. 067471-0017 10/051,335 CITATION IN AN APPLICATION **APPLICANT** TAKAYAMA, SHUICHI, et al. FILING DATE **GROUP** (PTO-1449) October 19, 2001 2191 **U.S. PATENT DOCUMENTS EXAMINER'S** CITE Document Number **Publication Date** Name of Patentee or Applicant of Cited Pages, Columns, Lines, Where **INITIALS** MM-DD-YYYY Relevant Passages or Relevant Document Number-Kind Code2 (if known) Figures Appear υs US FOREIGN PATENT DOCUMENTS **EXAMINER'S** Foreign Patent Document Publication Date Name of Patentee or Pages, Columns, Lines Translation INITIALS Applicant of Cited Document Where Relevant CITE Country Code3 - Number 4 - Kind MM-DD-YYYY Yes No Codes (if known) Figures Appear OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, **EXAMINER'S** INITIALS journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where CITE published. NO EDA, Hiroki. "News Reports: Intel and HP Unveiled Outline of Their Next Instruction Set "IA-64"" Nikkei Electronics (Nikkei Business Publications. Inc.) November 3, 1997, Number 702, pp. 27-28 KUMAGAI, Masayasu. " Chapter 4, Next Generation Pentium and Competing Processors, Details of VLIW and IA-64, and Comparisons with Alpha and PowerPC." Interface (CQ Publishing Co., Ltd.) March 1, 1998, Volume 24, Number 3, pp. 132-139 **EXAMINER** DATE CONSIDERED

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.